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Terms	Documents
L7 and (result same security same memory same order)	21

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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L10

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Recall Text Clear Interrupt

Search History

DATE: Tuesday, June 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L10	L7 and (result same security same memory same order)	21	L10
L9	L7 and (result same memory same order)	62	L9
L8	L7 and (result near10 order)	53	L8
L7	l1 and L6	245	L7
L6	execut$3 same (availab$5 or free)	51497	L6
L5	l1 and L4	1	L5
L4	(execution adj1 unit) same (availab$5 or free)	1469	L4
L3	l1 and L2	0	L3
L2	(distribut$3 or provid$3) same (execution adj1 unit) same (availab$5 or free)	142	L2
L1	request same security same memory	854	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L10	0

Database:
US Pre-Grant Publication Full-Text Database
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Search: L11

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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
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DB=USPT,USOC; PLUR=YES; OP=OR			
L10	L7 and (result same security same memory same order)	21	L10
L9	L7 and (result same memory same order)	62	L9
L8	L7 and (result near10 order)	53	L8
L7	l1 and L6	245	L7
L6	execut$3 same (availab$5 or free)	51497	L6
L5	l1 and L4	1	L5
L4	(execution adj1 unit) same (availab$5 or free)	1469	L4
L3	l1 and L2	0	L3
L2	(distribut$3 or provid$3) same (execution adj1 unit) same (availab$5 or free)	142	L2
L1	request same security same memory	854	L1

h e b b cg b e e ch

Freeform Search

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Term: L7 and (result same security same memory same order)

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Search History

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DB=USPT,USOC; PLUR=YES; OP=OR			
L10	L7 and (result same security same memory same order)	21	L10
L9	L7 and (result same memory same order)	62	L9
L8	L7 and (result near10 order)	53	L8
L7	l1 and L6	245	L7
L6	execut$3 same (availab$5 or free)	51497	L6
L5	l1 and L4	1	L5
L4	(execution adj1 unit) same (availab$5 or free)	1469	L4
L3	l1 and L2	0	L3
L2	(distribut$3 or provid$3) same (execution adj1 unit) same (availab$5 or free)	142	L2
L1	request same security same memory	854	L1

END OF SEARCH HISTORY

h e b b g e e e e gh c f ff e ch

Refine Search

Search Results -

Terms	Documents
(707/8 |717/149 |709/201 |710/22 |710/52 |710/39 |710/200 |711/163 |712/215 |712/221 |712/34 |713/200 |705/405).ccls.	6805

Database:
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- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
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- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, June 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count
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END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L2	29

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EPO Abstracts Database
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Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, June 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count
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L3	l1 and L2	29
L2	request same security same memory same execut$3	161
L1	710/22,52,39,200;713/200;711/163;712/215,221,34;705/405;707/8;709/201;717/149.ccls.	6805

END OF SEARCH HISTORY

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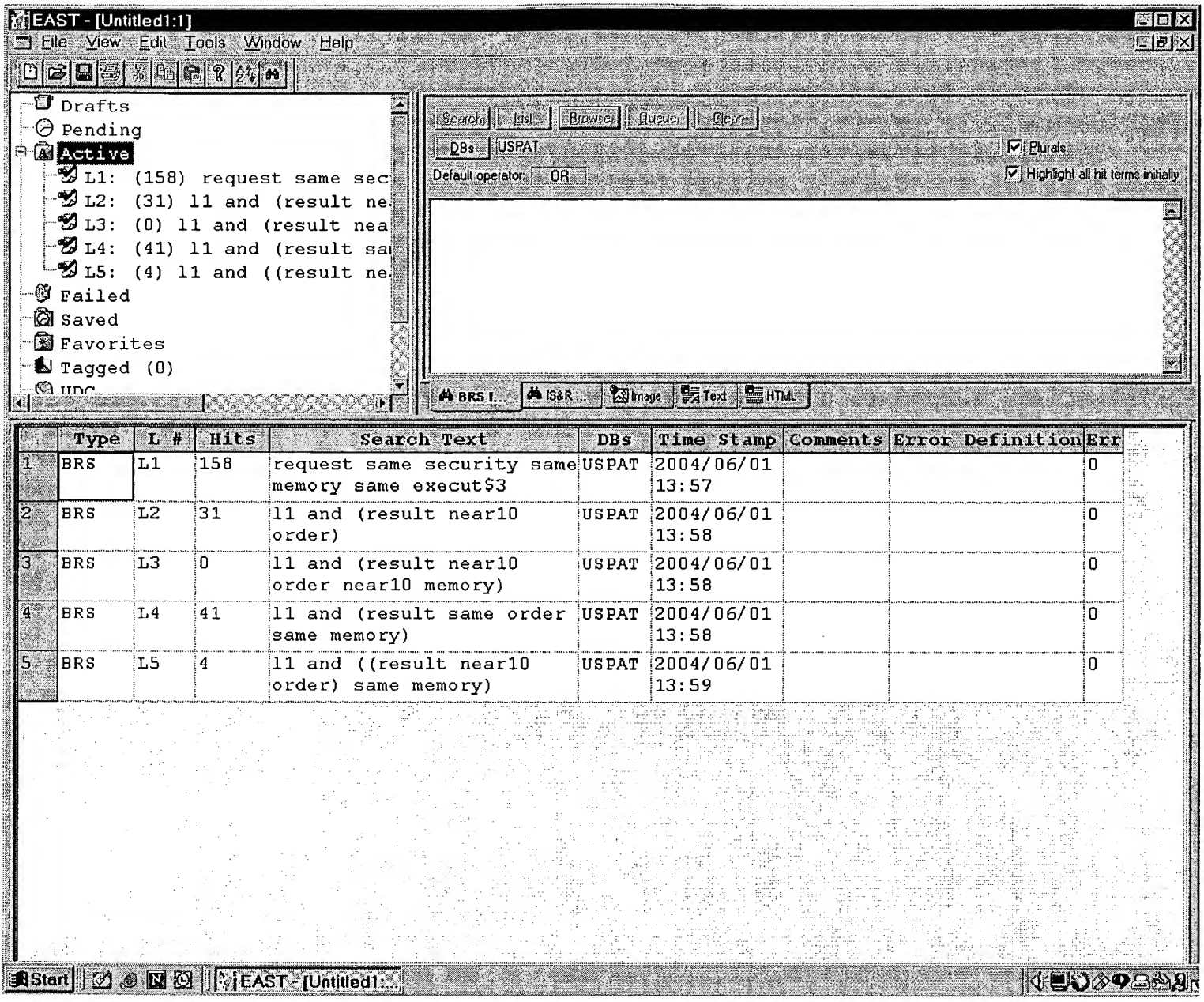

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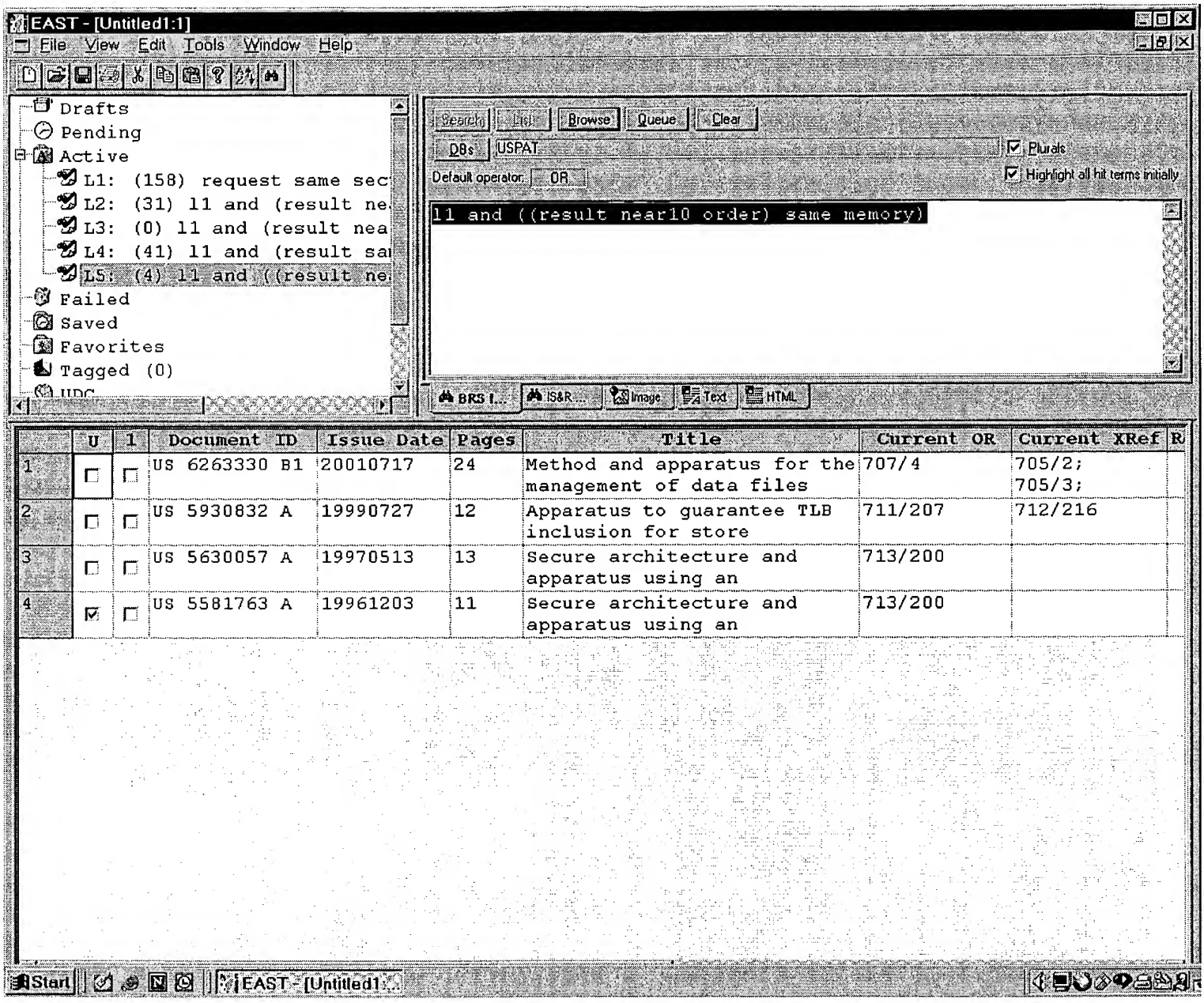
2	BRS	L2	31	l1 and (result near10 order)	USPAT	2004/06/01 13:58			0
3	BRS	L3	0	l1 and (result near10 order near10 memory)	USPAT	2004/06/01 13:58			0
4	BRS	L4	41	l1 and (result same order same memory)	USPAT	2004/06/01 13:58			0
5	BRS	L5	4	l1 and ((result near10 order) same memory)	USPAT	2004/06/01 13:59			0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Method and apparatus for the management of data files
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US 5930832 A
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Apparatus to guarantee TLB inclusion for store
711/207
712/216
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US 5630057 A
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US 5581763 A
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Results Key:
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1 **Multi-view memory to support OS locking for transaction systems**
Bodorik, P.; Jutla, D.N.;
Database Engineering and Applications Symposium, 1997. IDEAS '97. Proceedings., International , 25-27 Aug. 1997
Pages:309 - 318

[Abstract] [PDF Full-Text (924 KB)] **IEEE CNF**

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Multi-view memory to support OS locking for transaction systems

Bodorik, P. Jutla, D.N.
Fac. of Comput. Sci., Dalhousie Univ., Halifax, NS , Canada;

This paper appears in: **Database Engineering and Applications Symposium, 1997. IDEAS '97. Proceedings., International**

Meeting Date: 08/25/1997 - 08/27/1997
Publication Date: 25-27 Aug. 1997
Location: Montreal, Que. Canada
On page(s): 309 - 318
Reference Cited: 38
Number of Pages: xii+403
Inspec Accession Number: 5710441

Abstract:
The focus of this paper is to investigate the use of the multi-view **memory** (MVM) model and its supporting architecture in providing efficient locking services for transaction processing systems. The model provides for enforcement of access control protocols through FSM specification on units of data that can vary in size from one region of **memory** to another. Threads **executing** transactions do not explicitly **request** locks on data items-they simply access the data items while locking is performed automatically

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and in many instances without software intervention. This is facilitated by hardware assistance in that the FSM definitions and lock unit state information is stored in caches. Only when a thread is suspended are the state changes communicated to the software lock manager. Delays for lock acquisitions through the MVM model architecture are determined and compared to delays due to lock acquisition by a conventional lock manager

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Index Terms:
authorisation cache storage concurrency control database theory distributed databases finite state machines **memory** protocols network operating systems **security** of data storage management transaction processing FSM specification MVM model architecture OS locking access control protocols cache concurrency control delays finite state machines lock acquisition lock unit state information multi-view **memory** model operating system locking software lock manager threads transaction processing systems

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L10: Entry 15 of 21 File: USPT Sep 8, 1998

DOCUMENT-IDENTIFIER: US 5805711 A
TITLE: Method of improving the security of postage meter machines

Brief Summary Text (50):
The EPROM accepts the majority part of the program code and makes an external program code available to the microprocessor via the microprocessor bus. Since, however, the program variables are additionally stored in the internal OTP-RAM, a security-associated encapsulation of the program execution is achieved. Program executions having different security levels can thus be designationally realized with an OTP processor. A faulty or manipulated postage meter machine remains completely in the OTP-ROM with its program execution and cannot be forced into different operating modes.

Detailed Description Text (13):
A start security check routine is undertaken, which checks the most important, externally maintained postage meter machine data and external program code completely encapsulated in the internal ROM and RAM area of the OTP with its program code. This security check routine can thereby recognize manipulations--without an external possibility of influencing with manipulative intent thereby existing--that had been implemented during the deactivated condition of the postage meter machine and can then effectively inhibit further operation of the postage meter machine if the check routines are not run error-free. In this case, the program execution remains in an endless program loop in the OTP-ROM (error handing 1030). The external storage media are used by the MP (read EPROM, write RAM) only after the checks have been run error-free and the system routine 200 is reached.

Detailed Description Text (94):
The control unit 6 is a microprocessor or an OTP processor. In addition to a microprocessor, non-volatile memories and further circuits are accommodated in a common housing in the OTP. The internal, non-volatile memory, for example, includes program memories and, in particular, also allows the possibility of setting security bits that prevent the read-out of the internal non-volatile memory toward the outside. These security bits are set in the OTP during the manufacture of the postage meter machine. Following such security-associated routines such as, for example, accounting routines with an emulator/debugger would likewise lead to a modified time execution which can be identified by the OTP processor. This also includes a clock generator/counter circuit for the prescription of time intervals or clock cycles, for example, for the time-out generation or printer control. When a specific time has elapsed and the anticipated event has not occurred, the clock generator/counter circuit generates an interrupt that reports the result-free expiration of the time span to the microprocessor, whereupon the microprocessor initiates further measures. Inventively, the clock generator/counter circuit is utilized for monitoring program running time. A known number of clock cycles for the program execution of predetermined program parts is thereby used. Before the start of the routine, the counter of the clock generator/counter circuit is pre-set or reset in a predetermined way. After the start of the program routine, the counter reading is continuously modified corresponding to the clock pulses of the clock generator. After processing the critical, predetermined program parts, the status of the counter is interrogated by the microprocessor and is compared to the anticipated value. When a predetermined deviation in the running time of critical

or, respectively, security-associated program parts is exceeded, the postage meter machine can thus no longer be operated for franking (kill mode 1). When a manipulator performs an unauthorized operation, the postage meter machine is effectively shut down during the running time by being converted into the first mode.

Detailed Description Text (96):
During times in which printing is not carried out (standby mode) that an inquiry ensues in view of manipulation attempts and/or the checksum of the register readings is formed and/or is formed over the content of the program memory PSP 11. In order to improve the security against manipulation, the checksum is thereby formed for a kill mode 2 in the OTP over the content of the external program memory PSP 11 and the result is compared to a predetermined value stored in the OTP. This preferably ensues in step 101 when the postage meter machine is started or in step 213 when the postage meter machine is operated in standby mode. The standby mode is reached when a predetermined time elapses without an input or a print request. The latter occurs when a letter sensor of a known type--not shown in detail--does not identify a next envelope that is to be franked. Step 405--shown in FIG. 5--in the franking mode 400 therefore also includes a further inquiry about a time lapse, whereby a time transgression ultimately leads again to point e, and thus to the input routine according to step 209. When the interrogation criterion is met, a standby flag is set in step 408 and a direct branch is made back to the point s to the system routine 200 or the point t without running through the accounting and printing routine in step 406. The standby flag is interrogated later in step 211 and is reset in step 213 after the checksum check when no manipulation attempt has been recognized.

Detailed Description Text (98):
In order to further enhance the security against manipulations, a flow control is inventively utilized that is set forth below. Such a flow control ensues by modifying a numerical value in a memory at at least one point during the implementation of the program routine. After the execution of the program routine, the modified numerical value is compared to a predetermined numerical value allocated to this program routine. When branchings are executed during the program run, different numerical values will result. A plausibility test is implemented in a following evaluation or a determination can be made as to what branchings were executed. This is achieved by the modification of the numerical value ensuing by a multiplication by a specific prime number allocated to the respective program part. A prime number resolution merely has to be implemented then in a later evaluation.

First Hit Fwd Refs

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L10: Entry 15 of 21 File: USPT Sep 8, 1998

US-PAT-NO: 5805711
DOCUMENT-IDENTIFIER: US 5805711 A

TITLE: Method of improving the security of postage meter machines

DATE-ISSUED: September 8, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Windel; Harald	Berlin			DE
Reisinger; Frank	Berlin			DE
Freytag; Claus	Berlin			DE
Kubatzki; Ralf	Berlin			DE
Hansel; Marcus	Berlin			DE
Gunther; Stephan	Berlin			DE
Bischoff; Enno	Berlin			DE
Wagner; Andreas	Berlin			DE
Zarges; Olav A.	Berlin			DE
Berthold; Arndt	Berlin			DE
Rieckhoff; Peter	Berlin			DE

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Francotyp-Postalia AG & Co.	Birkenwerder			DE	03

APPL-NO: 08/ 525923 [PALM]
DATE FILED: September 8, 1995

PARENT-CASE:
RELATED APPLICATION The present application is a continuation-in-part of U.S. application Ser. No. 08/346,909 filed Nov. 30, 1994 ("Method for Improving the Security of Postage Meter Machines," Windel et al.), filed under the provisions of 37 C.F.R. .sctn.1.53, now U.S. Pat. No. 5,671,146.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	43 44 476.8	December 21, 1993

INT-CL: [06] H04 L 9/00

US-CL-ISSUED: 380/55; 380/2, 380/4, 380/23, 380/25, 380/49, 380/50, 380/51, 705/401, 705/405, 705/408, 705/410
US-CL-CURRENT: 380/55; 380/2, 380/51, 705/401, 705/405, 705/408, 705/410, 705/60, 713/187

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FIELD-OF-SEARCH: 380/2, 380/4, 380/23, 380/24, 380/25, 380/49, 380/50, 380/51, 380/55, 380/59, 364/464.11, 364/464.14, 364/464.15, 705/401, 705/405, 705/408, 705/410

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3255439	June 1966	Simjian	
☐	4129302	December 1978	Stone	
☐	4251874	February 1981	Check, Jr.	
☐	4347506	August 1982	Duwel et al.	
☐	4549281	October 1985	Eckert et al.	
☐	4746234	May 1988	Harry	
☐	4785417	November 1988	Obrea	
☐	4811234	March 1989	Storace	
☐	4812965	March 1989	Taylor	
☐	4812994	March 1989	Taylor et al.	
☐	4864506	September 1989	Storace	
☐	5077660	December 1991	Haines et al.	
☐	5181245	January 1993	Jones	
☐	5243654	September 1993	Hunter	
☐	5572429	November 1996	Hunter et al.	364/464.14
☐	5638442	June 1997	Gargiulo et al.	380/2

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 388 840	September 1990	EP	
0 388 839	September 1990	EP	
0 194 660	March 1992	EP	
0 516 403	December 1992	EP	
0 547 922	June 1993	EP	
0 576 113	December 1993	EP	
0 578 042	January 1994	EP	
0 647 925	April 1995	EP	
2 233 937	January 1991	GB	

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"Asymmetrische Verschlusselung auf der Chipkarte," Drews et al., Design & Elektronik vol. 4, Feb. 16, 1993, pp. 76-81.
"Damit Geheimdaten vertraulich bleiben--Verschlusselungsalgorithmus IDEA lost DES ab," Bruggemann et al., Elektronik, vol. 10 (1993) pp 84-93.

ART-UNIT: 362

PRIMARY-EXAMINER: Gregory; Bernarr E.

ABSTRACT:

A method for securing data and program code of an electronic postage meter machine against manipulation, having a microprocessor in a control unit of the postage meter machine for implementing steps for a start and initialization routine and following system routine with a possibility of entering into a communication mode with a remote data central, as well as further input steps in order to enter into a franking mode from which a branch is made back into the system routine after the implementation of an accounting and printing routine, includes conducting a start security check within the framework of a start and initialization routine which runs before a secure printing data call routine and the following system routine for determining the validity of a program code and/or of data in the predetermined memory location and of an appertaining MAC (message authentification code) that is present in the same storage medium. The check for valid program code and/or for validity of the data is implemented with a selected checksum method within an OTP (one time programmable) processor that internally receives the corresponding program parts. Transfer of the postage meter machine into the aforementioned system routine takes place given validity of the data or transfer of the postage meter machine into a first mode when the data are invalid, or when a specific manipulation criterion is met. Steps for preventing the franking or blocking of the postage meter machine and/or steps for preventing a further program execution or a program branch exiting the OTP processor within the framework of system routine the occur.

18 Claims, 15 Drawing figures

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L12: Entry 3 of 4 File: USPT Mar 17, 1998

DOCUMENT-IDENTIFIER: US 5729729 A
TITLE: System for fast trap generation by creation of possible trap masks from early trap indicators and selecting one mask using late trap indicators

Abstract Text (1):
An improved method and apparatus for ordering traps in a multiscalar design to avoid pipeline delays. Execution units which generate their traps earlier in the pipeline are used to build a number of possible enable masks, for indicating which instructions should complete, using the ordering information available from the different execution units. The enable masks cover the different possibilities of trap or no trap for the execution units which produce later traps. The traps from the execution units providing a later trap indication then select from the possible enable masks depending upon whether or not a trap is indicated by such second group of execution units. The enable mask is then used to enable or disable the destination registers used by the different execution units for that group of instructions.

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L12: Entry 3 of 4 File: USPT Mar 17, 1998

US-PAT-NO: 5729729
DOCUMENT-IDENTIFIER: US 5729729 A

TITLE: System for fast trap generation by creation of possible trap masks from early trap indicators and selecting one mask using late trap indicators

DATE-ISSUED: March 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Leung; Arthur T.	Sunnyvale	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 08/ 664477 [PALM]
DATE FILED: June 17, 1996

INT-CL: [06] G06 F 9/00

US-CL-ISSUED: 395/591; 395/565
US-CL-CURRENT: 712/244; 712/224

FIELD-OF-SEARCH: 395/591, 395/565, 395/569

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3883851	May 1975	Drake et al.	395/565
☐	5193158	March 1993	Kinney et al.	395/591
☐	5237700	August 1993	Johnson et al.	395/591
☐	5341482	August 1994	Cutler et al.	395/591
☐	5481685	January 1996	Nguyen et al.	395/591

ART-UNIT: 235

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PRIMARY-EXAMINER: Ellis; Richard L.

ATTY-AGENT-FIRM: Townsend and Townsend and Crew LLP

ABSTRACT:

An improved method and apparatus for ordering traps in a multiscalar design to avoid pipeline delays. Execution units which generate their traps earlier in the pipeline are used to build a number of possible enable masks, for indicating which instructions should complete, using the ordering information available from the different execution units. The enable masks cover the different possibilities of trap or no trap for the execution units which produce later traps. The traps from the execution units providing a later trap indication then select from the possible enable masks depending upon whether or not a trap is indicated by such second group of execution units. The enable mask is then used to enable or disable the destination registers used by the different execution units for that group of instructions.

20 Claims, 4 Drawing figures

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L12: Entry 3 of 4 File: USPT Mar 17, 1998

US-PAT-NO: 5729729
DOCUMENT-IDENTIFIER: US 5729729 A

TITLE: System for fast trap generation by creation of possible trap masks from early trap indicators and selecting one mask using late trap indicators

DATE-ISSUED: March 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Leung; Arthur T.	Sunnyvale	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 08/ 664477 [PALM]
DATE FILED: June 17, 1996

INT-CL: [06] G06 F 9/00

US-CL-ISSUED: 395/591; 395/565
US-CL-CURRENT: 712/244; 712/224

FIELD-OF-SEARCH: 395/591, 395/565, 395/569

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3883851	May 1975	Drake et al.	395/565
☐	5193158	March 1993	Kinney et al.	395/591
☐	5237700	August 1993	Johnson et al.	395/591
☐	5341482	August 1994	Cutler et al.	395/591
☐	5481685	January 1996	Nguyen et al.	395/591

ART-UNIT: 235

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PRIMARY-EXAMINER: Ellis; Richard L.

ATTY-AGENT-FIRM: Townsend and Townsend and Crew LLP

ABSTRACT:

An improved method and apparatus for ordering traps in a multiscalar design to avoid pipeline delays. Execution units which generate their traps earlier in the pipeline are used to build a number of possible enable masks, for indicating which instructions should complete, using the ordering information available from the different execution units. The enable masks cover the different possibilities of trap or no trap for the execution units which produce later traps. The traps from the execution units providing a later trap indication then select from the possible enable masks depending upon whether or not a trap is indicated by such second group of execution units. The enable mask is then used to enable or disable the destination registers used by the different execution units for that group of instructions.

20 Claims, 4 Drawing figures

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L5: Entry 1 of 1 File: USPT Jul 27, 1999

US-PAT-NO: 5930832
DOCUMENT-IDENTIFIER: US 5930832 A

TITLE: Apparatus to guarantee TLB inclusion for store operations

DATE-ISSUED: July 27, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heaslip; Jay Gerald	Williston	VT		
Herzl; Robert Dov	South Burlington	VT		
Tran; Arnold Steven	South Burlington	VT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 08/ 660560 [PALM]
DATE FILED: June 7, 1996

INT-CL: [06] G06 F 12/10

US-CL-ISSUED: 711/207; 395/392
US-CL-CURRENT: 711/207; 712/216

FIELD-OF-SEARCH: 395/392, 395/390, 711/207

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5191649	March 1993	Cadambi et al.	395/200
☐	5206945	April 1993	Nishimukai et al.	395/425
☐	5226126	July 1993	McFarland et al.	395/375
☐	5283886	February 1994	Nishii et al.	395/425
☐	5564111	October 1996	Glew et al.	395/185.06

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OTHER PUBLICATIONS

Computer Dictionary. Second Edition. Microsoft Press. 1994. p. 377.
Superscalar Microprocessor Design. Michael Johnson. Prentice Hall. 1991. pp. 26-28 and 50-53.
IBM Technical Disclosure Bulletin, "Special Serialization for "Load-with-Update" Instruction to Reduce the Complexity of Register Renaming Circuitry", vol. 37, No. 10, Oct. 1994, pp. 59-60.

ART-UNIT: 271

PRIMARY-EXAMINER: Chan; Eddie P.

ASSISTANT-EXAMINER: Verbrugge; Kevin

ATTY-AGENT-FIRM: Murray; Susan Abate; Joseph P.

ABSTRACT:

A computer system includes a processor and a cache and memory management unit. The processor includes a means for retiring instructions in program order. The cache and memory management unit includes means for detecting when a translation has been evicted from a lookaside buffer and means for communicating eviction information to the means for retiring instructions in program order. The means for retiring instructions in program order includes means for holding a storage related instruction which causes a miss in the lookaside buffer or in the cache in a first pass of execution until the instruction becomes the oldest storage related instruction in program sequence and further includes means responsive to the eviction information for flushing all storage related instructions except the current storage related instruction. The system avoids the occurrence of misses in the buffer late in execution (e.g., PASS 2 or later), thus avoiding a necessity for complex recovery provisions.

6 Claims, 8 Drawing figures

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L5: Entry 1 of 1 File: USPT Jul 27, 1999

US-PAT-NO: 5930832
DOCUMENT-IDENTIFIER: US 5930832 A

TITLE: Apparatus to guarantee TLB inclusion for store operations

DATE-ISSUED: July 27, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heaslip; Jay Gerald	Williston	VT		
Herzl; Robert Dov	South Burlington	VT		
Tran; Arnold Steven	South Burlington	VT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 08/ 660560 [PALM]
DATE FILED: June 7, 1996

INT-CL: [06] G06 F 12/10

US-CL-ISSUED: 711/207; 395/392
US-CL-CURRENT: 711/207; 712/216

FIELD-OF-SEARCH: 395/392, 395/390, 711/207

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5191649	March 1993	Cadambi et al.	395/200
☐	5206945	April 1993	Nishimukai et al.	395/425
☐	5226126	July 1993	McFarland et al.	395/375
☐	5283886	February 1994	Nishii et al.	395/425
☐	5564111	October 1996	Glew et al.	395/185.06

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OTHER PUBLICATIONS

Computer Dictionary. Second Edition. Microsoft Press. 1994. p. 377.
Superscalar Microprocessor Design. Michael Johnson. Prentice Hall. 1991. pp. 26-28 and 50-53.
IBM Technical Disclosure Bulletin, "Special Serialization for "Load-with-Update" Instruction to Reduce the Complexity of Register Renaming Circuitry", vol. 37, No. 10, Oct. 1994, pp. 59-60.

ART-UNIT: 271

PRIMARY-EXAMINER: Chan; Eddie P.

ASSISTANT-EXAMINER: Verbrugge; Kevin

ATTY-AGENT-FIRM: Murray; Susan Abate; Joseph P.

ABSTRACT:

A computer system includes a processor and a cache and memory management unit. The processor includes a means for retiring instructions in program order. The cache and memory management unit includes means for detecting when a translation has been evicted from a lookaside buffer and means for communicating eviction information to the means for retiring instructions in program order. The means for retiring instructions in program order includes means for holding a storage related instruction which causes a miss in the lookaside buffer or in the cache in a first pass of execution until the instruction becomes the oldest storage related instruction in program sequence and further includes means responsive to the eviction information for flushing all storage related instructions except the current storage related instruction. The system avoids the occurrence of misses in the buffer late in execution (e.g., PASS 2 or later), thus avoiding a necessity for complex recovery provisions.

6 Claims, 8 Drawing figures

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US006263330B1

(12) **United States Patent**
Bessette

(10) **Patent No.: US 6,263,330 B1**
(45) **Date of Patent: Jul. 17, 2001**

(54) **METHOD AND APPARATUS FOR THE MANAGEMENT OF DATA FILES**

(76) Inventor: Luc Bessette, 201-50 de Brésoles, Montréal (CA), H2Y 1V5

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/087,843

(22) Filed: May 29, 1998

(30) **Foreign Application Priority Data**

Feb. 24, 1998 (CA) 2231019
Apr. 1, 1998 (CA) 2233794

(51) Int. Cl.[7] G06F 17/30

(52) U.S. Cl. 707/4; 707/10; 707/100; 707/102; 707/104; 709/203; 705/2; 705/3

(58) Field of Search 707/4, 3, 10, 100, 707/102, 104; 709/203; 705/2, 3

(56) **References Cited**

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(List continued on next page.)

Primary Examiner—John Breene
Assistant Examiner—Cheryl Lewis
(74) *Attorney, Agent, or Firm*—Ratner & Prestia

(57) **ABSTRACT**

The present invention provides a network system for storage of medical records. The records are stored in a database on a server. Each record includes two main parts, namely a collection of data elements containing information of medical nature for the certain individual, and a plurality of pointers providing addresses or remote locations where reside other medical data for that particular individual. Each record also includes a data element indicative of the basic type of medical data found at the location pointed to by a particular pointer. This arrangement permits a client workstation to download the record along with the set of pointers which link the client to the remotely stored files. The identification of the basic type of information that each pointer points to allows the physician to select the ones of interest and thus avoid downloading massive amounts of data where only part of that data is needed at that time. In addition, this record structure allows statistical queries to be effected without the necessity of accessing the data behind the pointers. For instance, a query can be built based on keys, one of which is the type of data that a pointer points to. The query can thus be performed solely on the basis of the pointers and the remaining information held in the record.

15 Claims, 12 Drawing Sheets

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US005630057A

United States Patent [19]

Hait

[11] Patent Number: 5,630,057

[45] Date of Patent: May 13, 1997

[54] SECURE ARCHITECTURE AND APPARATUS USING AN INDEPENDENT COMPUTER CARTRIDGE

[75] Inventor: John N. Hait, Missoula, Mont.

[73] Assignee: Progressive Technology Inc., Missoula, Mont.

[21] Appl. No.: 677,324

[22] Filed: Jul. 1, 1996

Related U.S. Application Data

[63] Continuation of Ser. No. 155,240, Apr. 29, 1994, Pat. No. 5,581,763, which is a continuation of Ser. No. 513,415, Apr. 23, 1990, abandoned, which is a continuation-in-part of Ser. No. 206,001, Jun. 14, 1988, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/186

[58] Field of Search 395/186, 700

[56] References Cited

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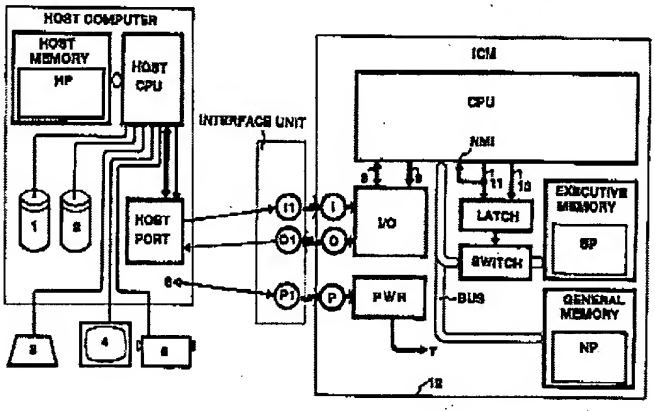
5,438,674	8/1995	Keele et al.	395/404
5,497,479	3/1996	Hornbuckle	395/461

Primary Examiner—Kevin A. Kriess
Assistant Examiner—John I. Chavis
Attorney, Agent, or Firm—Leonard D. Schappert

[57] ABSTRACT

A computer architectural and apparatus system for preventing software copying or alteration, and providing enhanced computational capabilities, physical information security, and physical environment protection is disclosed. The system comprises an Independent Computer Module (ICM), and an Interface Unit. The ICM comprises a CPU, a RAM, a ROM, a memory switching means, a communications port, and a connectorless interface contained within a sealed cartridge. The Interface Unit comprises a receptacle for receiving the ICM, which contains a matching connectorless interface, and wiring to a host computer's port and power. The connectorless interface uses directional electromagnetic emitters and sensors to prevent signal leakage. The memory switching means turns off the entire secure memory, enabling non-secure programs to be run from another section of RAM. Reactivation of secure memory by a non-secure program causes program control to be transferred to a fixed address within the secure program.

15 Claims, 3 Drawing Sheets



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US005930832A

United States Patent [19]

Heaslip et al.

[11] Patent Number: 5,930,832

[45] Date of Patent: Jul. 27, 1999

[54] **APPARATUS TO GUARANTEE TLB INCLUSION FOR STORE OPERATIONS**

[75] Inventors: **Jay Gerald Heaslip**, Williston; **Robert Dov Herzl**; **Arnold Steven Tran**, both of South Burlington, all of Vt.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **08/660,560**

[22] Filed: **Jun. 7, 1996**

[51] **Int. Cl.**[6] **G06F 12/10**

[52] **U.S. Cl.** **711/207**; 395/392

[58] **Field of Search** 395/392, 390; 711/207

[56] **References Cited**

U.S. PATENT DOCUMENTS

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5,226,126	7/1993	McFarland et al.	395/375
5,283,886	2/1994	Nishii et al.	395/425
5,564,111	10/1996	Glew et al.	395/185.06

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Computer Dictionary. Second Edition. Microsoft Press. 1994. p. 377.

Superscalar Microprocessor Design. Michael Johnson. Prentice Hall. 1991. pp. 26–28 and 50–53.

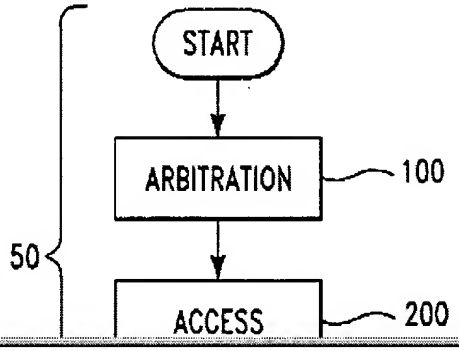
IBM Technical Disclosure Bulletin, "Special Serialization for "Load-with-Update" Instruction to Reduce the Complexity of Register Renaming Circuitry", vol. 37, No. 10, Oct. 1994, pp. 59–60.

Primary Examiner—Eddie P. Chan
Assistant Examiner—Kevin Verbrugge
Attorney, Agent, or Firm—Susan Murray; Joseph P. Abate

[57] **ABSTRACT**

A computer system includes a processor and a cache and memory management unit. The processor includes a means for retiring instructions in program order. The cache and memory management unit includes means for detecting when a translation has been evicted from a lookaside buffer and means for communicating eviction information to the means for retiring instructions in program order. The means for retiring instructions in program order includes means for holding a storage related instruction which causes a miss in the lookaside buffer or in the cache in a first pass of execution until the instruction becomes the oldest storage related instruction in program sequence and further includes means responsive to the eviction information for flushing all storage related instructions except the current storage related instruction. The system avoids the occurrence of misses in the buffer late in execution (e.g., PASS 2 or later), thus avoiding a necessity for complex recovery provisions.

6 Claims, 6 Drawing Sheets



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Search Results -

Terms	Documents
5953502.pn. or 6295645.pn. or 6373846.pn. or 6378072.pn.	4

Database:
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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
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IBM Technical Disclosure Bulletins

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Search History

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DB=USPT; PLUR=YES; OP=OR			
L1	5953502.pn. or 6295645.pn. or 6373846.pn. or 6378072.pn.	4	L1

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Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6378072 B1

L1: Entry 1 of 4 File: USPT Apr 23, 2002

US-PAT-NO: 6378072
DOCUMENT-IDENTIFIER: US 6378072 B1
** See image for Certificate of Correction **

TITLE: Cryptographic system

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 2. Document ID: US 6373846 B1

L1: Entry 2 of 4 File: USPT Apr 16, 2002

US-PAT-NO: 6373846
DOCUMENT-IDENTIFIER: US 6373846 B1

TITLE: Single chip networking device with enhanced memory access co-processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 3. Document ID: US 6295645 B1

L1: Entry 3 of 4 File: USPT Sep 25, 2001

US-PAT-NO: 6295645
DOCUMENT-IDENTIFIER: US 6295645 B1

TITLE: Method and apparatus for providing downloadable functionality to an embedded coprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 4. Document ID: US 5953502 A

L1: Entry 4 of 4 File: USPT Sep 14, 1999

US-PAT-NO: 5953502

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DOCUMENT-IDENTIFIER: US 5953502 A

TITLE: Method and apparatus for enhancing computer system security

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
5953502.pn. or 6295645.pn. or 6373846.pn. or 6378072.pn.	4

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L1: Entry 4 of 4 File: USPT Sep 14, 1999

US-PAT-NO: 5953502
DOCUMENT-IDENTIFIER: US 5953502 A

TITLE: Method and apparatus for enhancing computer system security

DATE-ISSUED: September 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Helbig, Sr.; Walter A	Medford Lakes	NJ	08055	

US-CL-CURRENT: 713/200; 714/36

ABSTRACT:

A security enhanced computer system arrangement includes a coprocessor and a multiprocessor logic controller inserted into the architecture of a conventional computer system. The coprocessor and multiprocessor logic controller is interposed between the CPU of the conventional computer system to intercept and replace control signals that are passed over certain of the critical control signal lines associated with the CPU. The multiprocessor logic controller arrangement thereby isolates the CPU of the conventional computer system from the remainder of the conventional computer system, permitting separate control over the CPU and separate control over the remainder of the computer system. By controlling the control signals that are normally passed between the CPU and the remainder of the computer system, the multiprocessor logic controller permits the coprocessor to perform highly secure operations. These secure operations, selectable by a trusted operator or built in to a cooperating operating system, verify that the computer system is a trusted computing base which can be relied upon to perform its operations properly and without compromise.

70 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

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